

What is claimed is:

1. A data processor comprising:

an electrically erasable or programmable program  
memory;

5 a central processing unit capable of accessing  
the program memory; and

malfunction exclusion means for excluding a  
malfunction due to occurrence of an interrupt during  
erasing or programming of the data in the program  
10 memory.

2. A data processor comprising:

an electrically erasable or programmable program  
memory;

a central processing unit capable of accessing  
15 the program memory;

a storage circuit for realizing random access by  
the central processing unit; and

control circuit for moving a part of the storage  
means to a vector address area of the program memory  
20 in accordance with an interrupt request generated  
during erasing or programming of the data in the  
program memory.

3. A data processor comprising:

an electrically erasable or programmable program  
25 memory;

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a central processing unit capable of accessing the program memory;

a storage circuit for realizing random access by the central processing unit; and

5 a control circuit for moving the vector address area of the program memory to the storage means in accordance with an interrupt request generated during erasing or programming of the data in the program memory.

10 4. A data processor comprising:

an electrically erasable or programmable program memory;

a central processing unit capable of accessing the program memory; and

15 a control logic circuit for excluding an interrupt request to the central processing unit during erasing or programming of the data in the program memory in accordance with a request for erasing or programming the data in the program memory.

20 5. A data processor comprising:

an electrically erasable or programmable program memory;

a central processing unit capable of accessing the program memory; and

25 a control logic circuit for stopping the

processing for erasing or programming the data in the  
program memory in response to an interrupt request  
generated to the central processing unit during  
erasing or programming of the data in the program  
5 memory in accordance with a request for erasing or  
programming the data in the program memory.